REMARKS

These remarks are in reply to the Office Action mailed June 13, 2006. Claims 1-42 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat. to Wollan et al.[1] ("Wollan").

Claims 1-7, 10-18, 21-29, 32-33, and 37-42 have been amended to clarify the claimed subject matter. In addition, claims 8-9, 19-20, 30-31, and 34-36 have been cancelled. Applicant respectively traverses the rejections.

Amended independent claims 1 and 23 provide for producing first and second counts of address-bytes received. In addition, these claims recite selecting first and second registers corresponding respectively with the first and second counts. Amended independent claims 12 and 37 recite "an address-byte-received counter to count address-bytes received on the bus" and "a selecting unit to select one of the at least two registers according to the count of the address-byte-received counter." Claims 1, 12, 23, and 37, as amended, each recite that each register is "associated with a particular count of address-bytes received on the bus."

In contrast, Wollan discloses a watchdog timer, timer counters, and a program counter. The watchdog timer counts an oscillator signal and when a delay time has elapsed asserts an MCU reset signal.[2] While little is said about them, the timer counters presumably also count time. The program counter receives signals from an instruction decoder and specifies program instructions.[3] (The instruction decoder decodes fetched instructions and produces signals for incrementing the program counter.[4]) Thus, the program "counter" merely performs addition or subtraction operations (as opposed to counting) in accord with various signals in order to specify a next instruction.[5] Therefore, with respect to the watchdog timer, timer counters, and a program counter, Wollan does not disclose counting address-bytes received. Nor does Wollan disclose a counter for counting address-bytes received. Moreover, Wollan does not disclose selecting a register that is associated with a particular count of address-bytes received.

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[1] No. 5,809,327
[2] Col. 18, lines 10-27. See Figure 11.
[3] Col. 4, lines 33-34. See Figure 9.
[4] Col. 10, lines 1-10.
[5] One of ordinary skill in the art will appreciate that an instruction counter may also be referred to an instruction sequencer or an instruction pointer.

The Wollan reference discloses that a pair of 8-bit registers may be provisioned as a logical sixteen bit register. The logical sixteen bit register is used as an indirect address register pointer for RAM and program-space addressing. Certain arithmetic operations on the contents of the logical register are provided, such as incrementing operations.[6] These arithmetic operations are performed by logic unit ALU-2.[7] In the previous Office Actions, the Examiner maintained that, with respect to claim 1 for example, the step of (c) incrementing a count as a result of receiving one byte is taught by this disclosure. However, incrementing the *content* of a logical register is not equivalent to incrementing a count whenever a byte is received.

In the previous Office Actions, the Examiner also maintained that, again with respect to claim 1, a step of (d) *addressing* one of the two registers according to the incremented count is taught by the disclosure of a logical sixteen bit register used as an indirect address register pointer. However, Wollan discloses that individual 8-bit registers are addressed using "the WE_XH, WE_XL, WE_YH, WE_YL, WE_ZH, and WE_ZL control lines" from selector control circuitry 134.[8] Thus, Wollan fails to disclose addressing a register according to an incremented count of bytes received.

It may be assumed, for sake of argument, that Wollan discloses addressing a register according to an incremented count of bytes received. However, even under this assumption, Wollan does not anticipate the claimed invention. For example, amended claim 37 recites both registers and memory. A selecting unit uses a count of address-bytes received on a bus to determine which register to select and address-bytes define memory locations. Similarly, Wollan discloses registers and a RAM. But selector control circuitry determines which register to select and the ALU-2 defines RAM locations. Thus, even it is assumed for sake of argument that the logic circuit recited in claim 37corresponds to the ALU-2, Wollan does not anticipate claim 37. The reason is that the claimed logic circuit selects a register, but the ALU-2 selects a location in a RAM.

[6] Col. 5, lines 11-16.
[7] Col. 5, lines 23-23.
[8] See Fig. 3.

Accordingly, the Wollan reference fails to disclose each and every element of independent claims 1, 12, 23, and 37. Each of the dependent claims depends from one of these independent claims. The dependent claims are not anticipated for the same reason that the independent claims are not anticipated.

Conclusion

The Wollan reference fails to disclose each and every element of any of the claims. Therefore, Wollan does not anticipate any of the claims. Accordingly, claims 1-7, 10-18, 21-29, 32-33, and 37-42 are in condition for allowance. Applicant respectfully requests that these claims be allowed, and this application be passed to issue. If the Examiner feels that a telephone interview would be helpful, she is respectfully invited to call applicant's attorney, Richard Wilhelm (48,786) at 503-635-1187.

Respectfully submitted,

/Mark P. Watson/
Mark P. Watson
Registration No. 31,448

Please address all correspondence to:

Epson Research and Development, Inc.
Intellectual Property Department
2580 Orchard Parkway, Suite 225
San Jose, CA 95131
Phone: (408) 952-6124
Facsimile: (408) 954-9058
Customer No. 20178

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